

BINGHAM McCUTCHEN

Facsimile

DATE January 9, 2004

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TO	Examiner Matthew C. Dooley United States Patent and Trademark Office	703-746-8183	703-306-5538

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FROM Jeffrey S. Smith (650) 849-4800 (650) 849-4422
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PAGES (INCLUDING THIS COVER PAGE): 6

RE U.S. Application Serial No.: 09/765,958

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Per our conversation this morning. Please confirm receipt of this fax by return fax or call Sheila Henriquez @ 650-849-4455, or email at sheila.henriquez@bingham.com.

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DATE April 22, 2003

	NAME	FAX	PHONE
TO	Examiner Magid Dimyan U.S. Patent & Trademark Office	703/872-9318	

FROM Jeffrey S. Smith (650) 849-4800 (650) 849-4422
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PAGES (INCLUDING THIS COVER PAGE): 4

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TO	Examiner Magid Dimyan U.S. Patent & Trademark Office	703/872-9318	

FROM	Jeffrey S. Smith jeffrey.smith@bingham.com	(650) 849-4800	(650) 849-4422
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Appl. No. 09/765,958

261/085

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/765,958
Applicant: Bulent Dervisoglu, Laurence H. Cooke
Filing Date: 1/18/01
Title: Hierarchical Test Circuit Structure for Chips with Multiple Circuit Blocks
Assignee: Cadence Design Systems, Inc.
Examiner: Magid Dimyan
Group Art Unit: 2857
Docket No.: 261/085

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

7
Sir:

Before examination on the merits, please amend this application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 3 of this paper.